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ISP110x Eval Kit User Manual for the HVQFN14/16 Package

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Info	Content
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Abstract	The ISP110x eval board helps you to evaluate the features of the ISP110x. This document explains the evaluation of the ISP110x for the HVQFN14 and HVQFN16 packages. *Notes*: ISP110x denotes the ISP1102, ISP1104, ISP1105 and ISP1106 Philips Advanced Universal Serial Bus transceivers, and any future derivatives.

PHILIPS

Revision history

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2.0	Mar 2004	Removed ISP1107
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Contact information

For additional information, please visit: *http://www.semiconductors.philips.com/*

For sales office addresses, please send an email to: *sales.addresses@www.semiconductors.philips.com*

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Note: ISP110x denotes the ISP1102, ISP1104, ISP1105, and ISP1106 Philips Advanced Universal Serial Bus transceivers, and any future derivatives.

1. ISP110x Eval Board

1.1. Objective

The ISP110x evaluation (eval) board helps you to evaluate the features of the ISP110x.

This document explains the evaluation of the ISP110x for the HVQFN14 and HVQFN16 packages, which are cheaper than the HBCC16 package.

1.2. Description

The ISP110x is a generic Universal Serial Bus (USB) transceiver integrated circuit (IC) that is compliant with *Universal Serial Bus Specification Rev. 2.0*. It operates linearly from 3.3 V to 5.0 V, and is backward compatible with Philips' PDIUSBP11A.

Both the PDIUSBP11A and the ISP110x support two types of driver interfaces: the Philips encoded data interface and the USB-IF standard data interface. This compatibility allows greater flexibility in designs and applications.

To facilitate testing, all the ISP110x pins are connected to one side of the JP7 and JP12 headers. The other side is connected to the ground. Some ISP110x pins, such as MODE, $\overline{OE}$, SUSPND, VMO/FSE0, VPO/VO, SOFTCON and SPEED, are pulled up using 1 MΩ resistors.

Jumper settings can be used to configure transceivers and capacitors for characterization functions.

The mode of operating the eval board depends on the IC used, as well as some jumpers' settings for signaling requirement.

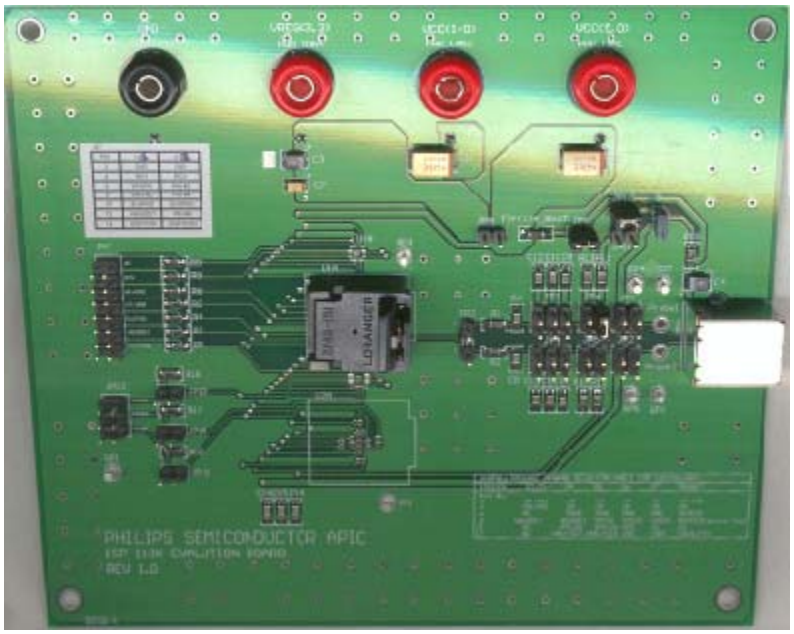

Figure 1-1: ISP110x Eval Kit for the HVQFN14 and HVQFN16 Packages

Table 1-1 shows the signal contents of headers and their corresponding signal names in the ISP110x.

Table 1-1: Signal Contents of Headers and their Corresponding Signal Names in the ISP110x

Header	Signal	In			
		ISP1102	ISP1104	ISP1105	ISP1106
JP7	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
	RCV	RCV	RCV	RCV	RCV
	VP	VP/VPO	VP	VP	VP
	VM	VM/VMO	VM	VM	VM
	SUSPEND	SUSPEND	SUSPEND	SUSPEND	SUSPEND
	SPEED	VBUSDET	VBUSDET	SPEED	SPEED
	SOFTCON	SOFTCON	SOFTCON	SOFTCON	SOFTCON
JP12	Pin 6	No connection	MODE	MODE	GND
	Pin 12	No connection	VMO/FSE0	VMO/FSE0	VMO
	Pin 11	No connection	VPO/VO	VPO/VO	VPO

Table 1-2 shows the jumper settings on the eval board.

Table 1-2: Jumper Settings

Jumper	Setting
JP1	Sharing mode or pull-down to GND on D+
JP2	Sharing mode or pull-down to GND on D-
JP3	Different capacitor leads for characterized testing on D+
JP4	Different capacitor leads for characterized testing on D-
JP5	1.5 kΩ pull-up or 15 kΩ pull-down on D-
JP6	1.5 kΩ pull-up or 15 kΩ pull-down on D+
JP8	Short $V_{CC(5.0)}$ to $V_{reg(3.3)}$
JP9	Connect to the V_{BUS} line
JP10	For back drive voltage purpose
JP11	Connect to $V_{pu(3.3)}$
JP13	Connect to HVQFN16 pin 6
JP14	Connect to HVQFN16 pin 12
JP15	Connect to HVQFN16 pin 11

2. Mode Selection for Applications

Table 2-1: Mode Selection for the HVQFN16 Package

IC Products and Packages	Connection	Operation Mode
ISP1102	No connection	Differential Input Mode (VO/VPO, VM/VMO)—Bidirectional
ISP1104	Short JP12[1] and JP13	Single-Ended Input Mode (VO, FSE0)
	Short JP13	Differential Input Mode (VPO, VMO)
ISP1105	Short JP12[1] and JP13	Single-Ended Input Mode (VO, FSE0)
	Short JP13	Differential Input Mode (VPO, VMO)
ISP1106	Short JP12[1] and JP13	Differential Input Mode (VPO, VMO)

[1] Use jumper on pins 1 and 2.

3. Power Supply Configurations

The ISP110x can be used with different power supply configurations by setting jumpers JP1, JP2, JP3 and JP4. These jumpers are used to suit the power supply application environment, as shown in Table 3-1.

Table 3-1: Power Supply Configurations

Mode	Environment	Connected Voltages	Jumpers Required	Remarks
Normal	+5.0 V operation (self-powered)	$V_{CC(5.0)}$ $V_{CC(I/O)}$	Not applicable	Connect $V_{CC(5.0)}$ to a 5 V source (4.0 V to 5.5 V) Connect $V_{CC(I/O)}$ to 1.65 V to 3.6 V range of the backend logic circuit (or external supply voltage)
	Bus-powered operation (V_{BUS} line)	V_{BUS} line	JP9	Connect to the V_{BUS} line (*Note*: Does not need any external source.)
	+3.3 V operation (bypass mode)	$V_{CC(5.0)}$ $V_{reg(3.3V)}$ $V_{CC(I/O)}$	JP8	$V_{CC(5.0)}$ and $V_{reg(3.3V)}$ are shorted and connected to a 3.3 V source Connect $V_{CC(I/O)}$ to 1.65 V to 3.6 V range of the backend logic circuit (external supply voltage)
Disable	+5.0 V operation (self-powered)	$V_{CC(5.0)}$	Not applicable	Connect $V_{CC(5.0)}$ to a 5 V source (4.0 V to 5.5 V) (*Note*: No $V_{CC(I/O)}$ is connected to the source.)
Sharing		$V_{CC(I/O)}$	Not applicable	Connect only $V_{CC(I/O)}$ to 1.65 V to 3.6 V range of the backend logic circuit (external supply voltage) (*Note*: $V_{CC(5.0)}$ and $V_{reg(3.3V)}$ are not connected to the source)

The ISP1102, ISP1105, and ISP1106 transceivers have a regulator bypass mode, in which $V_{CC(5.0)}$ can be connected to $V_{reg(3.3)}$ with a maximum voltage drop of 0.3 V (2.7 V to 3.6 V). The ISP1104 transceiver does not support this mode.

The ISP1102 and ISP1104 transceivers do not support the disable mode.

In the default setting (the normal bus-powered mode configuration), there are jumpers—JP9, JP11 and JP6—on pins 3 and 4.

4. Function Testing

4.1. Function Selection

Table 4-1: Function Table[1]

SUSPND	$\overline{OE}$	RCV	VP/VM	D+ and D-	Remarks
LOW	LOW	Active	Active	Active	Driving and receiving (differential receiver active)
HIGH	LOW	Inactive[2]	Active	Active	Driving during suspend (differential receiver inactive)[3]
LOW	HIGH	Active	Active	Hi-Z	Receiving only[4]
HIGH	HIGH	Inactive[2]	Active	Hi-Z[4]	Low-power state

[1] Active = HIGH; Inactive = LOW.
[2] In the suspend mode (SUSPND = HIGH), the differential receiver is inactive and output RCV is always LOW. Out-of-suspend ('K') signaling is detected through the single-ended receivers VP and VM.
[3] During suspend, the slew-rate control circuit of the low-speed operation is disabled. The D+ and D- lines are still driven to their intended states, without the slew-rate control. This is permitted because driving during suspend is used to signal remote wake-up by driving a 'K' signal (one transition from idle to the 'K' state) for a period of 1 ms to 15 ms.
[4] Signal levels on D+ and D- are determined using other USB devices and external pull-up and pull-down resistors.

4.2. Driver Interface Selection for ISP1104; ISP1105; ISP1106

Table 4-2: Driving Function

Mode	VPO/VO	VMO/FSE0	Data	Interface
0	LOW	LOW	Differential 0	Philips Encoded Data Interface
	LOW	HIGH	SE0	
	HIGH	LOW	Differential 1	
	HIGH	HIGH	SE0	
1	LOW	LOW	SE0	USB-IF Standard Data Interface
	LOW	HIGH	Differential 0	
	HIGH	LOW	Differential 1	
	HIGH	HIGH	Illegal Data	

Table 4-3: Driving Function using the Single-Ended Input Data Interface ($\overline{OE}$ = LOW) [for ISP1104 and ISP1105 (MODE = LOW)]

FSE0	VO	DATA
LOW	LOW	Differential logic 0
LOW	HIGH	Differential logic 1
HIGH	LOW	SE0
HIGH	HIGH	SE0

Table 4-4: Driving Function using the Differential Input Data Interface ($\overline{OE}$ = LOW)

[for ISP1104, ISP1105 and ISP1106 (MODE = HIGH)]

VMO	VPO	DATA
LOW	LOW	SE0
LOW	HIGH	Differential logic 1
HIGH	LOW	Differential logic 0
HIGH	HIGH	Illegal state

Table 4-5: Receiving Function ($\overline{OE}$ = HIGH)

D+ and D-	RCV	VP[1]	VM[1]
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV*[2]	LOW	LOW

[1] VP = VM = 'HIGH' indicates the sharing mode ($V_{CC(5.0)}$ is disconnected).
[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is kept stable during the SE0 period.

4.3. Driver Interface Selection for the ISP1102

Table 4-6: Driving Function using the Differential Input Data Interface ($\overline{OE}$ = LOW)

[for ISP1102 Transmitting Function]

VM/VMO	VP/VPO	DATA
LOW	LOW	SE0
LOW	HIGH	Differential logic 1
HIGH	LOW	Differential logic 0
HIGH	HIGH	Illegal state

Table 4-7: Driving Function using the Differential Input Data Interface ($\overline{OE}$ = HIGH)

[for ISP1102 Receiving Function]

VM/VMO	VP/VPO	DATA
LOW	LOW	SE0
LOW	HIGH	Differential logic 1
HIGH	LOW	Differential logic 0
HIGH	HIGH	Illegal state

Table 4-8: Receiving Function ($\overline{OE}$ = HIGH)

(D+, D-)	RCV	VP[1]	VM[1]
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV*[2]	LOW	LIGH

[1] VP/VPO = 'HIGH' and VM/VMO = 'HIGH' indicate the sharing mode ($V_{CC(5.0)}$ is disconnected).
[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is kept stable during the SE0 period.

5. Schematic of the ISP110x HVQFN14 and HVQFN16 Packages

Depending on the application, Table 5-1 and Table 5-2 provide guidelines for setting up the ISP110x HVQFN14 and HVQFN16 packages, respectively.

Table 5-1: Setting up the ISP110x HVQFN14 Package (U1A/B)

Pin No	*Pin Name*	*ISP1102*
1	#OE	#OE
2	RCV	RCV
3	VP/VPO	VP/VPO
4	VM/VMO	VM/VMO
5	SUSPND	SUSPND
7	VBUSDET	VBUSDET
14	SOFTCON	SOFTCON

Table 5-2: Setting up the ISP110x HVQFN16 Package (U2A/B)

Pin No	*ISP1102*	ISP1104	*ISP1105*	*ISP1106*
6	No connection	*MODE*: Differential: when JP13 is used Single-ended: when JP12 and JP13 are used	*MODE*: Differential: when JP13 is used Single-ended: when JP12 and JP13 are used	*MODE*: JP13 and JP12
8	Not applicable	Not applicable	*SPEED*: full-speed; low-speed (when JP7 is used)	*SPEED*: full-speed; low-speed (when JP7 is used)
	VBUSDET[1]	VBUSDET[1]	Not applicable	Not applicable
4	VM/VMO	VM	VM	VM
3	VP/VPO	VP	VP	VP
11	No connection	VPO/VO	VPO/VO	VPO
12	No connection	VMO/FSE0	VMO/FSE0	VMO

[1] The VBUSDET pin is a V_{BUS} output indicator. When V_{BUS} is greater than 4.1 V, output is HIGH. When V_{BUS} is lower than 3.6 V, output is LOW. This feature is only applicable to the ISP1102 and the ISP1104.

6. Bill of Materials for the ISP110x Eval Board

Table 6-1: Bill of Materials

Description	Reference	Value	Quantity
Power supply plugs	PWR_Con1, PWR_Con2, PWR_Con3, PWR_Con4	CON	4
Tantalum capacitors	C14, C15, C16	18 pF	3
Electrolytic capacitor	C4	10 F	1
Electrolytic capacitor	C3	4.7 F	1
Electrolytic capacitors	C1, C2	47 F	2
Electrolytic capacitor	C7, C20, C21, C22, C23	1 F	5
Tantalum capacitors	C5, C6	33 pF	2
Tantalum capacitors	C10, C11	150 pF	2
Tantalum capacitors	C8, C9	47 pF	2
Tantalum capacitors	C12, C13	560 pF	2
Probes	TP1, TP2	—	2
Test Pin	GP1, GP2, GP3, GP4, GP5, GP6, GP7	-	7
Header	JP7	7 X 2	1
Header	JP12	3 X 2	1
Header	JP3, JP4	3 X 2	2
Header	JP1, JP2, JP5, JP6	2 X 2	4
Jumpers	JP8, JP9, JP10, JP11, JP13, JP14, JP15	—	7
Resistors	R5 to R9, R16 to R18	1 MΩ	10
Resistors	R11, R12	1.5 kΩ	2
Resistors	R13, R14	15 kΩ	2
Resistors	R1, R2	33 Ω	2
Resistors	R15	56 kΩ	1
Ferrite bead	Ferrite_bead1 (at 135MHz)	—	1
UP_CONN	CON1 (B Type)	—	1
MOSFET P (ZVN2106)	Q1	—	1
ISP110x_HVQFN14	U1B	—	1
ISP110x_HVQFN14_Socket	U1A	—	1
ISP110x_HVQFN16	U2B	—	1
ISP110x_HVQFN16_Socket	U2A	—	1

7. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1102 Advanced Universal Serial Bus transceiver* data sheet
- *ISP1104 Advanced Universal Serial Bus transceiver* data sheet
- *ISP1105_1106 Advanced Universal Serial Bus transceivers* data sheet.